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09/832,232	04/10/2001	Tomohiko Yamamoto	55801 (70904)	8972

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EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2674	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,232	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-59* is/are pending in the application.

4a) Of the above claim(s) *28-3032-34, 36, 37 and 54-59* is/are withdrawn from consideration.

5)☒ Claim(s) *5* is/are allowed.

6)☐ Claim(s) *2-4,6-9,16,17,19-22,24-27 and 44-53* is/are rejected.

7)☒ Claim(s) *10-13 and 38-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 2-13, 16, 17, 19-22, 24-27 and 38-53, drawn to gray scale capability (halftone), classified in class 345, subclass 89.

Group II. Claims 28-30, 32-34, 36, 37 and 54-59, drawn to data signal compensation in response to temperature, classified in class 345, subclass 101.

The inventions are distinct, each from the other because: Group I, which is drawn to gray scale capability (halftone), can function independently from Group II, which is drawn to data signal compensation in response to temperature.

Inventions Group I and Group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as Group II. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with William J. Daley, Jr. (Reg. No. 35,487) on May 25, 2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 2-13, 16, 17, 19-22, 24-27 and 38-53. Affirmation of this

election must be made by applicant in replying to this Office action. Claims 28-30, 32-34, 36, 37 and 54-59 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2, 3, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent # 6,577,295 ("Kikkawa")

Regarding claim 2, Kikkawa teaches a potential difference between the pixel electrode 17 and the common electrode 15 is 5 volts. In FIG. 10, each voltage of the electrodes is calculated for the case that voltage Vd of the scanning line 13 is 21 volts in an on-state and -8 volts in an off-state thereof, voltage Vd of the signal line 14 is 12 volts in a positive voltage frame period and 2 volts in a negative voltage frame period, and voltage Vcom of the common electrode 15 is fixed at 6 volts(column 7, lines 15-22). The prior art does specifically teaches the signal lines becomes different depending on the polarities. However, the prior art teaches in a negative voltage frame period, a potential difference of 5 volts having a polarity opposite to the polarity in the positive voltage frame period is generated between the common electrode 15 and the pixel electrode 17, to generate the desired parallel electric field 100 (column 4,

lines 6-13). It would have been obvious to one or ordinary skill in the art to modify the signal lines becomes different depending on the polarities to achieve a negative voltage frame period, a potential difference of 5 volts having a polarity opposite to the polarity in the positive voltage frame period is generated between the common electrode 15 and the pixel electrode 17, to generate the desired parallel electric field 100 .

Regarding claim 3, Kikkawa teaches a potential difference between the pixel electrode 17 and the common electrode 15 is 5 volts. In FIG. 10, each voltage of the electrodes is calculated for the case that voltage Vd of the scanning line 13 is 21 volts in an on-state and -8 volts in an off-state thereof, voltage Vd of the signal line 14 is 12 volts in a positive voltage frame period and 2 volts in a negative voltage frame period, and voltage Vcom of the common electrode 15 is fixed at 6 volts(column 7, lines 15-22) where the pulse Vg of Figure 10 is interpreted as the pulse width.

Regarding claim 6, Kikkawa teaches a potential difference between the pixel electrode 17 and the common electrode 15 is 5 volts. In FIG. 10, each voltage of the electrodes is calculated for the case that voltage Vd of the scanning line 13 is 21 volts in an on-state and -8 volts in an off-state thereof, voltage Vd of the signal line 14 is 12 volts in a positive voltage frame period and 2 volts in a negative voltage frame period, and voltage Vcom of the common electrode 15 is fixed at 6 volts (column 7, lines 15-22).

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent # 6,577,295 ("Kikkawa") in view of US Patent # 5,847,687 ("Hirakata et al.").

Regarding claim 4, Kikkawa teaches a potential difference between the pixel electrode 17 and the common electrode 15 is 5 volts. In FIG. 10, each voltage of the electrodes is calculated for the case that voltage Vd of the scanning line 13 is 21 volts in an on-state and -8 volts in an off-state thereof, voltage Vd of the signal line 14 is 12 volts in a positive voltage frame period and 2 volts in a negative voltage frame period, and voltage Vcom of the common electrode 15 is fixed at 6 volts (column 7, lines 15-22). The prior art teaches all the claimed limitations as recited in claim 4 with the exception of providing the single scanning line is different for each polarity of the voltage applied to the pixel electrodes. However, Hirakata et al. teach the same scan line have different polarities (column 6, line 31). It would have been obvious to a person of ordinary skill in the art to utilize the teaching of Hirakata et al. in the active matrix LCD disclosed by Kikkawa because this would allow the reduction of the potential variation range of data while inverting the direction of electric fields applied to liquid crystal module.

4. Claims 7, 19, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (US Patent 6,359,607) in view of Yamaguchi et al. (US Patent Application 2003/0151573).

As to claim 7, Yanagi et al. discloses a method for driving an image display device, said method applying a voltage between a potential of signal lines (image signal voltage Vsp is applied to a pixel electrode, column 2, lines 27-28) and a potential of a common electrode counter potential VCOM, column 2, lines 47-48) when a potential of scanning lines is ON scanning voltage Vgh, column 2, lines 23-24, when TFT is ON

state, column 3, lines 44-45), and displaying tones by modulating a pulse width of a two-value voltage supplied to the signal lines (signal driver output with voltage levels Vsn and Vsp) wherein tones are displayed by shifting phases of waveforms of the signal lines and the scanning lines (waveform of Vs and Vg are out off phase as shown in figure 12), dot inversion (column 14, lines 24-30) but fails to teach displaying by pulse width modulation.

However, Yamaguchi et al. teach the time modulation means 12 first carries out pulse with modulation in one frame and controls the display tone level of each of the cells 41a, 41b, and 41c.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the method Yanagi et al. then apply pulse width modulation technique taught by Yamagichi et al., to obtain the method Yanagi et al. modified by Yamaguchi et al. because it will provide a cell generating means that may time-modulates the input signal levels to the respective cells.

As to claim 19, Yanagi et al. discloses a driving device (figure 9) of an image display device (column 2, lines 15-22) which includes a plurality of pixel electrodes (pixel electrode 103, column 1, lines 34-35) which are formed on a substrate (electrode substrate, column 1, lines 24-26), pixel switching elements which are individually connected to the pixel electrodes (switching element 102 composed of TFT connected to pixel electrodes, column 1, lines 3336), a plurality of signal lines for applying a data signal according to a display image to the pixel electrodes (image signal voltage Vsp is applied to a pixel electrode, column 2, lines 2728, plurality of signal lines S(1) through

S(n), column 1, lines 27-29, figure 9), and a common electrode for applying a common potential to pixels (counter electrode has a potential set to potential VCOM by counter electrode driving circuit COM , column 2, lines 32-34, figure 9). Yanagi et al. discloses said driving device applying a voltage between a potential of the signal lines (Vs shown in figure 11) and a potential of the common electrode when a potential of scanning lines is ON (figure 12 shows scanning pulse Vg). Yanagi et al. discloses phase shifting of waveform of scanning lines to the signal lines (Vg with respect to Vs shown in figure 12), polarity inversion (Vcom changes polarity periodically as shown in figure 17, dot inversion is well known, column 14, lines 24-30). Yanagi et al. fails to teach pulse width modulation.

However, Yamaguchi et al. teach the time modulation means 12 first carries out pulse with modulation in one frame and controls the display tone level of each of the cells 41a, 41b, and 41c.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the method Yanagi et al. then apply pulse width modulation technique taught by Yamagichi et al., to obtain the method Yanagi et al. modified by Yamaguchi et al. because it will provide a cell generating means that may time-modulates the input signal levels to the respective cells.

As to claim 24, see the same citation for claim 19 because claim 24 differs from claim 19 only in scope of image device. Note Yanagi et al. teaches image device (liquid crystal display device, column 1, lines 1-2).

5. Claims 8, 9, 20, 21, 25, 26, 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US Patent 6,504,521) in view of Hirai et al. (US Patent 5,874,933) and Ino et al. (US Patent 6,424,328).

As to claim 8, Inoue et al. discloses a method for driving an image display device (column 1, lines 6-7), said method applying a voltage between a potential of signal lines (signal line voltage V0, figure 17, column 7, lines 29-33) and a potential of a common electrode reference line drive voltage VCOM, column 7, lines 40-41) when a potential of scanning lines is ON (figure 17, TFT is switched ON, column 10, lines 7-8), and displaying tones by modulating a pulse width of a two-value voltage supplied to the signal lines (voltage levels VOA/VOB shown in figure 17) wherein tones are displayed by shifting phases of waveforms of the signal lines and the common electrode (waveforms of signal lines VOA/VOB versus Vcom are out off phase as shown in figure 17), teaches polarity inversion (Vcom is polarity and a common electrode for applying a common potential to pixels (common electrode 76, column 1, lines 35-36), sid driving device applying a voltage between a potential of the signal lines (signal voltage all applying VOA/VOB shown in figure 17) and a potential of the common electrode when a potential of scanning lines is ON (figure 12 shows scanning pulse Vg) . Inoue et al. teaches a signal line driving section for supplying a signal (drive circuit for generating signal line drive voltage, column 3, lines 22-25), phase shifting of waveform of counter electrode and waveform of signal lines (figure 17 shows phase shift of Vcom and signal line voltage VOA/VOB) but fails to teach pulse width modulation.

Hirai et al. discloses that pulse width modulation technique is well known (column 2, lines 1116). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the method Inoue et al. then apply pulse width modulation technique taught by Hirai et al., to obtain the apparatus Inoue et al. modified by Hirai et al. because it will provide a display with many gradation levels. Inoue et al. modified by Hirai et al. fails to teach polarity inversion. Ino et al. discloses that dot inversion is well known in the art (column 1, lines 20-22). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the apparatus Inoue et al. modified by Hirai et al. then apply pulse width modulation technique taught by Hirai et al., dot inversion as taught by Ino et al. to obtain the apparatus Inoue et al. modified by Hirai et al. and Ino et al. because it will improve image quality as taught by Ino et al. (column 1, line 23).

As to claim 9, Inoue et al. discloses a method for driving an image display device (column 1, lines 6-7), said method applying a voltage between a potential of signal lines (signal line voltage V0, figure 17, column 7, lines 29-33) and a potential of a common electrode reference line drive voltage VCOM, column 7, lines 40-41) when a potential of scanning lines is ON (figure 17, TFT is switched ON, column 10, lines 7-8), and displaying tones by modulating a pulse width of a two-value voltage supplied to the signal lines (voltage levels VOA/VOB shown in figure 17) wherein tones are displayed by shifting phases of waveforms of the signal lines and the common electrode (waveforms of signal lines VOA/VOB versus Vcom are out off phase as shown in figure 17), teaches polarity inversion (Vcom is polarity and a common electrode for applying a

common potential to pixels (common electrode 76, column 1, lines 35-36), sid driving device applying a voltage between a potential of the signal lines (signal voltage all applying VOA/VOB shown in figure 17) and a potential of the common electrode when a potential of scanning lines is ON (figure 12 shows scanning pulse Vg) . Inoue et al. teaches a signal line driving section for supplying a signal (drive circuit for generating signal line drive voltage, column 3, lines 22-25), phase shifting of waveform of counter electrode and waveform of signal lines (figure 17 shows phase shift of Vcom and signal line voltage VOA/VOB) but fails to teach pulse width modulation.

As to claim 20, Inoue et al. discloses a method for driving an image display device (column 1, lines 6-7), said method applying a voltage between a potential of signal lines (signal line voltage V0, figure 17, column 7, lines 29-33) and a potential of a common electrode reference line drive voltage VCOM, column 7, lines 40-41) when a potential of scanning lines is ON (figure 17, TFT is switched ON, column 10, lines 7-8), and displaying tones by modulating a pulse width of a two-value voltage supplied to the signal lines (voltage levels VOA/VOB shown in figure 17) wherein tones are displayed by shifting phases of waveforms of the signal lines and the common electrode (waveforms of signal lines VOA/VOB versus Vcom are out off phase as shown in figure 17), teaches polarity inversion (Vcom is polarity and a common electrode for applying a common potential to pixels (common electrode 76, column 1, lines 35-36), sid driving device applying a voltage between a potential of the signal lines (signal voltage all applying VOA/VOB shown in figure 17) and a potential of the common electrode when a potential of scanning lines is ON (figure 12 shows scanning pulse Vg) . Inoue et al.

teaches a signal line driving section for supplying a signal (drive circuit for generating signal line drive voltage, column 3, lines 22-25), phase shifting of waveform of counter electrode and waveform of signal lines (figure 17 shows phase shift of Vcom and signal line voltage VOA/VOB) but fails to teach pulse width modulation.

As to claim 21, see the same citation for claim 20 since claim 21 differs from claim 20 only in limitation scanning line driving section for varying an amplitude of a voltage supplied to scanning lines between positive application and negative application to positive side and negative side in voltage application to pixel electrodes with a reference voltage OV. Inoue et al. teaches polarity inversion of signal voltage and common electrode voltage (figure 17, abstract, column 4, lines 64-65), scanning line driver (gate driver 28 shown in figure 6) with scanning line voltage amplitude changes between high and low (figure 16). As to claim 25, see the same citation for claim 20 since claim 25 differs from claim 20 in scope of image device (Inoue et al., liquid crystal display device, column 6, lines 25-26). As to claim 26, see the same citation for claim 21 since claim 26 differs from claim 21 in scope of image device (Inoue et al., liquid crystal display device, column 6, lines 25-26).

As to claim 25, Inoue et al. discloses a method for driving an image display device (column 1, lines 6-7), said method applying a voltage between a potential of signal lines (signal line voltage V0, figure 17, column 7, lines 29-33) and a potential of a common electrode reference line drive voltage VCOM, column 7, lines 40-41) when a potential of scanning lines is ON (figure 17, TFT is switched ON, column 10, lines 7-8), and displaying tones by modulating a pulse width of a two-value voltage supplied to the

signal lines (voltage levels VOA/VOB shown in figure 17) wherein tones are displayed by shifting phases of waveforms of the signal lines and the common electrode (waveforms of signal lines VOA/VOB versus Vcom are out off phase as shown in figure 17), teaches polarity inversion (Vcom is polarity and a common electrode for applying a common potential to pixels (common electrode 76, column 1, lines 35-36), sid driving device applying a voltage between a potential of the signal lines (signal voltage all applying VOA/VOB shown in figure 17) and a potential of the common electrode when a potential of scanning lines is ON (figure 12 shows scanning pulse Vg) . Inoue et al. teaches a signal line driving section for supplying a signal (drive circuit for generating signal line drive voltage, column 3, lines 22-25), phase shifting of waveform of counter electrode and waveform of signal lines (figure 17 shows phase shift of Vcom and signal line voltage VOA/VOB) but fails to teach pulse width modulation.

As to claim 26, Inoue et al. discloses a method for driving an image display device (column 1, lines 6-7), said method applying a voltage between a potential of signal lines (signal line voltage V0, figure 17, column 7, lines 29-33) and a potential of a common electrode reference line drive voltage VCOM, column 7, lines 40-41) when a potential of scanning lines is ON (figure 17, TFT is switched ON, column 10, lines 7-8), and displaying tones by modulating a pulse width of a two-value voltage supplied to the signal lines (voltage levels VOA/VOB shown in figure 17) wherein tones are displayed by shifting phases of waveforms of the signal lines and the common electrode (waveforms of signal lines VOA/VOB versus Vcom are out off phase as shown in figure 17), teaches polarity inversion (Vcom is polarity and a common electrode for applying a

common potential to pixels (common electrode 76, column 1, lines 35-36), sid driving device applying a voltage between a potential of the signal lines (signal voltage all applying VOA/VOB shown in figure 17) and a potential of the common electrode when a potential of scanning lines is ON (figure 12 shows scanning pulse Vg) . Inoue et al. teaches a signal line driving section for supplying a signal (drive circuit for generating signal line drive voltage, column 3, lines 22-25), phase shifting of waveform of counter electrode and waveform of signal lines (figure 17 shows phase shift of Vcom and signal line voltage VOA/VOB) but fails to teach pulse width modulation.

As to claim 44, Hirai et al. teach the switch section 110 of the scanning driver circuit 102 and the switch section 113 of the signal driver circuit 103 are controlled by the polarity inversion signal (FR) so that the polarity thereof can be inverted during a predetermined period (column 10, lines 33-38). The features of this fourth embodiment is that the amplitude of the liquid crystal application voltage is switched for each mode by switching the voltage switch 1101 column 13, lines 19-22).

As to claim 45, Hirai et al. teach the switch section 110 of the scanning driver circuit 102 and the switch section 113 of the signal driver circuit 103 are controlled by the polarity inversion signal (FR) so that the polarity thereof can be inverted during a predetermined period (column 10, lines 33-38). The features of this fourth embodiment is that the amplitude of the liquid crystal application voltage is switched for each mode by switching the voltage switch 1101 column 13, lines 19-22).

As to claim 46, Hirai et al. teach he features of this fourth embodiment is that the amplitude of the liquid crystal application voltage is switched for each mode by

switching the voltage switch 1101 column 13, lines 19-22) where the amplitude of the liquid crystal display is inherently has a lower voltage upon the negative application.

As to claim 47, Hirai et al. teach he features of this fourth embodiment is that the amplitude of the liquid crystal application voltage is switched for each mode by switching the voltage switch 1101 column 13, lines 19-22) where the amplitude of the liquid crystal display is inherently has a lower voltage upon the negative application.

6. Claims 22, 27, 48, 49, 50, 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US Patent 6,504,521) in view of Hirai et al. (US Patent 5,874,933) and Ino et al. (US Patent 6,424,328) and Okada et al. (US Patent 5,621,426).

As to claim 22, differ from claim 20 in limitation scanning line driving section for varying an amplitude of a voltage supplied to scanning lines so that a resistance of a transistor for switching ON or OFF signal application from the signal lines to the pixels is increased with time from a beginning to an end of an application time of a single pixel. Inoue et al. teaches gate driver 28 (column 6, lines 64-65), TFT switching ON/OFF via gate voltage (figures 12a/b) but does not teach resistance of transistor. Okada et al. teaches TFT 95 as switching means column 6, lines 57-58) and resistance is increased with time from zero (switch ON) to 10 exp 6 (switch OFF) (figure 16). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the apparatus Inoue et al. modified by Hirai et al. and Ino et al. and implement the increase of resistance of a switch as taught by Okada et al. , to obtain the apparatus Inoue et al. modified by Hirai et al. Ino et al. and Okada et al. because it will help reduce through

current by regulating the rising characteristics of the switch as taught by Okada et al. (column 10, lines 61-63).

As to claim 50, Hirai et al. teach he features of this fourth embodiment is that the amplitude of the liquid crystal application voltage is switched for each mode by switching the voltage switch 1101 column 13, lines 19-22) where the amplitude of the liquid crystal display is inherently has a lower voltage upon the negative application.

As to claim 27, see the same citation for claim 22 because claim 27 differs from claim 22 in scope of image device. Note Inoue et al. teaches liquid crystal display device (column 6, lines 25-26).

As to claim 48, differ from claim 20 in limitation scanning line driving section for varying an amplitude of a voltage supplied to scanning lines so that a resistance of a transistor for switching ON or OFF signal application from the signal lines to the pixels is increased with time from a beginning to an end of an application time of a single pixel. Inoue et al. teaches gate driver 28 (column 6, lines 64-65), TFT switching ON/OFF via gate voltage (figures 12a/b) but does not teach resistance of transistor. Okada et al. teaches TFT 95 as switching means column 6, lines 57-58) and resistance is increased with time from zero (switch ON) to 10 exp 6 (switch OFF) (figure 16). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the apparatus Inoue et al. modified by Hirai et al. and Ino et al. and implement the increase of resistance of a switch as taught by Okada et al. , to obtain the apparatus Inoue et al. modified by Hirai et al. Ino et al. and Okada et al. because it will help reduce through

current by regulating the rising characteristics of the switch as taught by Okada et al. (column 10, lines 61-63).

As to claim 49, differ from claim 20 in limitation scanning line driving section for varying an amplitude of a voltage supplied to scanning lines so that a resistance of a transistor for switching ON or OFF signal application from the signal lines to the pixels is increased with time from a beginning to an end of an application time of a single pixel. Inoue et al. teaches gate driver 28 (column 6, lines 64-65), TFT switching ON/OFF via gate voltage (figures 12a/b) but does not teach resistance of transistor. Okada et al. teaches TFT 95 as switching means column 6, lines 57-58) and resistance is increased with time from zero (switch ON) to 10 exp 6 (switch OFF) (figure 16). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the apparatus Inoue et al. modified by Hirai et al. and Ino et al. and implement the increase of resistance of a switch as taught by Okada et al. , to obtain the apparatus Inoue et al. modified by Hirai et al. Ino et al. and Okada et al. because it will help reduce through current by regulating the rising characteristics of the switch as taught by Okada et al. (column 10, lines 61-63).

As to claim 52, differ from claim 20 in limitation scanning line driving section for varying an amplitude of a voltage supplied to scanning lines so that a resistance of a transistor for switching ON or OFF signal application from the signal lines to the pixels is increased with time from a beginning to an end of an application time of a single pixel. Inoue et al. teaches gate driver 28 (column 6, lines 64-65), TFT switching ON/OFF via gate voltage (figures 12a/b) but does not teach resistance of transistor. Okada et al.

teaches TFT 95 as switching means column 6, lines 57-58) and resistance is increased with time from zero (switch ON) to 10 exp 6 (switch OFF) (figure 16). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the apparatus Inoue et al. modified by Hirai et al. and Ino et al. and implement the increase of resistance of a switch as taught by Okada et al. , to obtain the apparatus Inoue et al. modified by Hirai et al. Ino et al. and Okada et al. because it will help reduce through current by regulating the rising characteristics of the switch as taught by Okada et al. (column 10, lines 61-63).

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. (US Patent 5,874,933) in view of Okada et al. (US Patent 5,621,426).

As to claim 16, Hirai et al. discloses a method for driving an image display device, said method displaying tones by modulating a pulse width of a two-value voltage supplied to the signal lines (pulse width modulation is well known technique in the art, column 2, lines 14-15) signal driver output with two-value voltage V3 and V5 as shown in figure 7) but does not teach resistance of a transistor. Okada et al. discloses a resistance of a transistor which switches ON or OFF signal application from the signal lines to pixels (switching element 95 as thin film transistor shown in figure 8) ; figure16 shows this resistance increases with time from a beginning to an end an application time of a single pixel, where the application time of the single pixel is one horizontal period (since TFT is a switching means, interval T1 shown in figure 16 corresponds to the claimed application time). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the method Hirai et al. for pulse width

modulation technique and switching the TFT via application of gate voltage as taught by Okada et al. to obtain the method Hirai et al. modified by Okada et al. because it will provide a multiple gradation display with reduced noise.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. (US Patent 5,874,933) in view of Okada et al. and Yanagi et al. (US Patent 6,359,607).

As to claim 17, Hirai et al. modified by Okada et al. fails to teach wherein the resistance of the transistor is varied by varying a gate voltage . Yanagi et al. discloses voltage-drain currency characteristic of the TFT, wherein a drain currency (ON resistance) linearly varies depending on gate voltage (column 7, lines 12-13). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize method Hirai et al. modified by Okada et al. then activate the scanning line connected to a TFT via variation gate voltage as taught by Yanagi et al. to obtain the method Hirai et al. modified by Okada et al. because it will reduce flickering and display defects, as taught by Yanagi et al. (column 8, lines 10-12).

As to claim 51, Hirai et al. teach he features of this fourth embodiment is that the amplitude of the liquid crystal application voltage is switched for each mode by switching the voltage switch 1101 column 13, lines 19-22) where the amplitude of the liquid crystal display is inherently has a lower voltage upon the negative application.

As to claim 53, Hirai et al. teach he features of this fourth embodiment is that the amplitude of the liquid crystal application voltage is switched for each mode by

switching the voltage switch 1101 column 13, lines 19-22) where the amplitude of the liquid crystal display is inherently has a lower voltage upon the negative application.

Allowable Subject Matter

9. Claim 5 is allowed over prior art.

10. Claims 10-13 and 38-43, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As to claims 10-11, none of prior art teaches a potential difference between the potential of the signal lines and the potential of the common electrode is maximum at an end of one horizontal period.

As to claims 12-13, none of prior art teaches a potential difference between the potential of the signal lines and the potential of the common electrode is minimum at an end of one horizontal period.

As to claims 38-43, none of the prior art teaches the potential of the signal lines is switched between the high level and low level after an elapsed time period which varies depending on the tone when the potential of the scanning lines is ON.

Response to Amendment

11. Applicant's arguments with respect to claims 2-13, 16, 17, 19-22, 24-27,and 38-53 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

112. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent	Okada et al.	5,592,190
U.S. Patent	Wakeland	5,892,496
U.S. Patent	Yoon	6,005,542
U.S. Patent	Moon	5,825,343
U.S. Patent	Iemoto et al.	5,300,945

Reference Okada et al. is made of record as it discloses a liquid crystal display apparatus with better temperature compensation .

Reference Wakeland is made of record as it discloses pulse width modulation technique.

Reference Yoon is made of record as it discloses a method for driving a thin film transistor liquid crystal display device.

Reference Moon is made of record as it discloses a driving device and method for a thin film transistor liquid crystal display.

Reference Iemoto et al. is made of record as it discloses a drive circuit for an active matrix display.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jean Lesperance whose telephone number is (571) 272-7692. The examiner can normally be reached on from Monday to Friday between 10:OOAM and 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art unit 2674

Date 5-26-2004

Henry N. Tran

HENRY N. TRAN
PRIMARY EXAMINER